CLAIMS

Having thus described the invention what is claimed as new and desired to be secured by Letters Patent is as follows:

1. An analog clock movement connectable to a power supply, said analog clock movement comprising:

a processor including a clock counter;

a correction-signal input connected to said processor;

a position sensor connected to said processor; and

a drive movement connected to said processor and associated with said position sensor.

2. The analog clock movement as claimed in Claim 1 wherein said correction-signal input comprises a carrier current receiver.

3. The analog clock movement as claimed in Claim 2 wherein said carrier current receiver comprises a plug-in frequency select module.

4. The analog clock movement as claimed in Claim 1 wherein said correction-signal input comprises a wired input.

5. The analog clock movement as claimed in Claim 1 wherein said correction-signal input comprises a carrier current receiver and a wired input.

6. The analog clock movement as claimed in Claim 1 wherein said drive movement comprises a quartz movement motor.

7. The analog clock movement as claimed in Claim 1 wherein the power supply comprises an alternating current.

8. The analog clock movement as claimed in Claim 7 wherein said clock counter uses said alternating current as a primary time base.

9. The analog clock movement as claimed in Claim 8 further comprising a quartz crystal associated with said clock counter as a secondary time base, and a reserve power supply connected to said crystal.

10. The analog clock movement as claimed in Claim 1 further comprising a quartz crystal associated with said clock counter as a time base.

11. The analog clock movement as claimed in Claim 1 further comprising a signal conditioner connected between said correction-signal input and said processor.

12. The analog clock movement as claimed in Claim 1 further comprising a reserve power supply connected to said processor.

13. The analog clock movement as claimed in Claim 12 wherein said reserve power supply comprises a capacitor.

14. The analog clock movement as claimed in Claim 1 wherein said position sensor comprises an optical sensor.

15. The analog clock movement as claimed in Claim 1 wherein said position sensor comprises a minute sensor and an hour sensor.

16. The analog clock movement as claimed in Claim 1 further comprising an options jumper connected to said processor.

17. The analog clock movement as claimed in Claim 1 further comprising a printed circuit board on which said processor, said position sensor and said drive motor are mounted.

18. The analog clock movement as claimed in Claim 17 wherein said printed circuit board comprises clock-face mounting points.

19. The analog clock movement as claimed in Claim 1 further comprising a system-status indicator connected to said processor.

20. The analog clock movement as claimed in Claim 19 wherein said system-status indicator comprises at least one light emitting diode.

21. The analog clock movement as claimed in Claim 1 further comprising a voltage regulator connected between said power supply and said processor.

22. A method of providing for time-correction of a secondary clock by a master clock including the steps of:

maintaining a clock counter within a secondary clock, said clock counter being independent of a master clock;

advancing a secondary clock movement in correspondence to said clock counter;

recognizing a time-correction signal generated by said master clock;

checking a movement position within said secondary clock in response to said time-correction signal;

comparing said movement position with a master-position indicated by said time-correction signal;

driving said movement to said master position upon an unequal comparison;

determining a time increment expended during said step of driving said movement to said master-position; and

forwarding said movement beyond said master-position by an amount corresponding to said determined time increment.

23. The method as claimed in Claim 22 wherein said clock counter comprises a primary time-base and a secondary time-base.

24. The method as claimed in Claim 23 further comprising the steps disabling said primary time-base and of maintaining said secondary time-base in the event of a power failure.

25. The method as claimed in Claim 22 further comprising the steps of:

suspending said advancing, recognizing, checking, comparing, driving, determining and forwarding steps during a power failure; and

maintaining a memory for said clock counter during said power failure.

26. The method as claimed in Claim 25 further comprising the steps of:

restoring said suspended operations upon restoration of power;

performing a memory test upon restoration of power; and

initiating advancement of said movement corresponding to said memory.

27. The method as claimed in Claim 22 wherein said step of recognizing a time-correction signal comprises the steps of:

ignoring an hourly time correction signal; and

recognizing a twelve hour time correction signal.

28. The method as claimed in Claim 22 further comprising the steps of:

suspending said maintaining, advancing, recognizing, comparing, determining and forwarding steps upon selection of a set-point option;

checking said movement position within said secondary clock;

comparing said movement position with a set-point position; and

driving said movement to said set-point position.

29. The method as claimed in Claim 22 further comprising the steps suspending all functions upon selection of a disable option.

30. An analog clock movement connectable to a power supply, said analog clock movement comprising:

a processor including a clock counter; and

a quartz movement motor connected to said processor.

31. The analog clock movement as claimed in Claim 30 further comprising a correction-signal input connected to said processor.

32. The analog clock movement as claimed in claim 30 further comprising a position sensor connected to said processor and associated with said motor.

33. The analog clock movement as claimed in Claim 30 further comprising a primary and a secondary time base.

34. The analog clock movement as claimed in Claim 33 further comprising a reserve power supply for said secondary time base.

35. The analog clock movement as claimed in Claim 30 wherein said quartz movement motor comprises an idler gear connecting a minute hand gear to a second hand gear.

36. An analog clock movement connectable to a power supply, said analog clock movement comprising:

a processor including a clock counter;

a primary time base and a secondary time base associated with said clock counter;

a correction-signal input connected to said processor;

a position sensor connected to said processor; and

a drive movement connected to said processor and associated with said position sensor.

37. The analog clock movement as claimed in Claim 36 wherein said primary time base comprises an alternating current and said secondary time base comprises a quartz crystal.

38. The analog clock movement as claimed in Claim 36 wherein said primary time base and said secondary time base comprise a quartz crystal.

39. The analog clock movement as claimed in Claim 36 further comprising a reserve power supply connected to said secondary time base.

40. A method of providing for time-correction of a secondary clock by a master clock including the steps of:

recognizing by a processor a time-correction signal;

determining by said processor if a clock movement is in a correct position;

initiating by said processor a high speed movement advancement upon an incorrect movement position;

terminating said high speed advancement upon a correct movement position.

41. The method as claimed in claim 40 further including the steps of:

ascertaining by said processor that said movement has reached a master-position; and

calculating by said processor a time increment expended during said high speed advancement to said master-position; and

forwarding said movement beyond said master-position by an amount corresponding to said calculated time increment.

42. An analog clock movement connectable to a power supply, said analog clock movement comprising:

a processor including a clock counter;

a correction-signal input connected to said processor;

a position sensor connected to said processor; and

a quartz drive movement connected to said processor and associated with said position sensor.

43. An analog clock movement connectable to a power supply, said analog clock movement comprising:

a processor including a clock counter;

a voltage pre-regulator connected to said processor;

a correction-signal input connected to said processor;

a position sensor connected to said processor; and

a drive movement connected to said processor and associated with said position sensor.